Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1 – 9: Cancelled

10. (currently amended) A circuit arrangement for bridging high voltages using a switching signal, comprising:

a voltage transmitter with first and second terminals for a low voltage;

a voltage receiver with third and fourth terminals for a higher voltage relative to the low voltage between the first and second terminals, wherein the voltage transmitter and the voltage receiver each comprise a first inverter circuit and a second inverter circuit,

wherein the inverter circuits of the voltage transmitter are connected between the first and second terminals and the inverter circuits of the voltage receiver are connected between the third and fourth terminals,

wherein an output ~~outlet~~ of the first inverter circuit of the voltage transmitter is connected via a first capacitor as a high voltage capacitor with an input ~~inlet~~ of the second inverter circuit of the voltage receiver and an output ~~outlet~~ of the first inverter circuit of the voltage receiver, and an output ~~outlet~~ of the second inverter circuit of the voltage transmitter is connected via a second capacitor as a high voltage capacitor with an input ~~inlet~~ of the first inverter circuit of the voltage receiver and an output ~~outlet~~ of the second inverter circuit of the voltage receiver,

wherein the inputs ~~inlets~~ of the first inverter circuit and the second inverter circuit, respectively, of the voltage transmitter are a non-inverted and an

inverted input ~~inlet~~, and wherein the outputs ~~outlets~~ of the first inverter circuit and the second inverter circuit, respectively, of the voltage receiver represent output ~~outlet~~ nodes,

wherein the circuit arrangement for bridging high voltage with a switching signal is realized as an integrated semi-conductor circuit made with semi-conductor processes with CMOS circuits as the inverter circuits or a stack of layers with alternating layers of circuit stopper implantation, field oxide, poly-silicon, CVD-oxide, metal, CVD-oxide, metal, and so on, whereby the layers are electrically alternatingly connected, as the first capacitor and as the second capacitor, respectively, as high voltage capacitors.

11. (currently amended)The circuit arrangement of claim 10, wherein a third inverter circuit is connected between the first and second terminals, wherein an output ~~outlet~~ of the third inverter circuit is connected with the input ~~inlet~~ of the first inverter circuit of the voltage transmitter, wherein the input ~~inlet~~ of the third inverter circuit is connected with the input ~~inlet~~ of the second inverter circuit of the voltage transmitter, and wherein the input ~~inlet~~ of the third inverter circuit is connected with a terminal IN as the input ~~inlet~~ of the circuit arrangement for bridging high voltages with a switching signal.

12. (currently amended)The circuit arrangement of claim 10, wherein a fourth inverter circuit and a fifth inverter circuit are connected between the third and fourth terminals, wherein an input ~~inlet~~ of the fourth inverter circuit is connected with the input ~~inlet~~ of the first inverter circuit of the voltage receiver, wherein an input ~~inlet~~ of the fifth inverter circuit is connected with the input ~~inlet~~ of the second inverter circuit of the voltage receiver, wherein an output ~~outlet~~ of the fourth inverter circuit is

connected with a terminal OUT1 as the first output ~~outlet~~ of the voltage receiver, and wherein an output ~~outlet~~ of the fifth inverter circuit is connected with a terminal OUT2 as the second output ~~outlet~~ of the voltage receiver.

13. (currently amended)The circuit arrangement of claim 11 ~~10~~, wherein a sixth inverter circuit and a seventh inverter circuit are connected between the first and second terminals, wherein an input ~~inlet~~ of the seventh inverter circuit is connected with the input ~~inlet~~ of the third inverter circuit and with a terminal IN as the input ~~inlet~~ of the circuit arrangement for bridging high voltages with a switching signal, wherein an output ~~outlet~~ of the seventh inverter circuit is connected with an input ~~inlet~~ of the sixth inverter circuit, and wherein an output ~~outlet~~ of the sixth inverter circuit is connected with the input ~~inlet~~ of the second inverter circuit of the voltage transmitter.

14. (previously presented) The circuit arrangement of claim 10, wherein an inverter circuit comprises two complementary transistors connected in series.

15. (currently amended) The circuit arrangement of claim 10, wherein the first capacitor and the second capacitor are connected between the voltage transmitter and the voltage receiver in such a way that the first capacitor and the second capacitor, respectively, are charged as high voltage capacitors to voltage differential to be overcome between the voltage transmitter and the voltage receiver and the charges of the first capacitor and second capacitor subsequently vary at a value $\Delta Q = C \times (Vdd - Vss)$ for signal transmission, wherein power consumption of the circuit arrangement for bridging high voltages with a switching signal is independent from the voltage differential to be overcome between the voltage transmitter and the voltage receiver, and wherein simultaneously, an ~~the~~ applied

differential principle in which C1 is charged at ΔQ, C2 is discharged at ΔQ, and vice versa guarantees a high signal-to-noise ratio relative to push-pull ~~push-push~~ interference signals.

16. (canceled)

17. (previously presented) The circuit arrangement of claim 10, wherein the voltage transmitter is one region or multiple regions of a semi-conductor chip, wherein the first capacitor is one region and the second capacitor is one region of the semi-conductor chip, wherein the voltage receiver is one region of the semi-conductor chip, wherein at least the region of the voltage transmitter and of the voltage receiver, respectively, is surrounded by a trench for voltage isolation.

18. (previously presented) The circuit arrangement of claim 10, wherein the circuit arrangement for bridging high voltages with a switching signal is realized as integrated semi-conductor circuits made with semi-conductor processes for integrated high voltage circuits with any isolation for the voltage transmitter, the high voltage capacitors, and the voltage receiver.